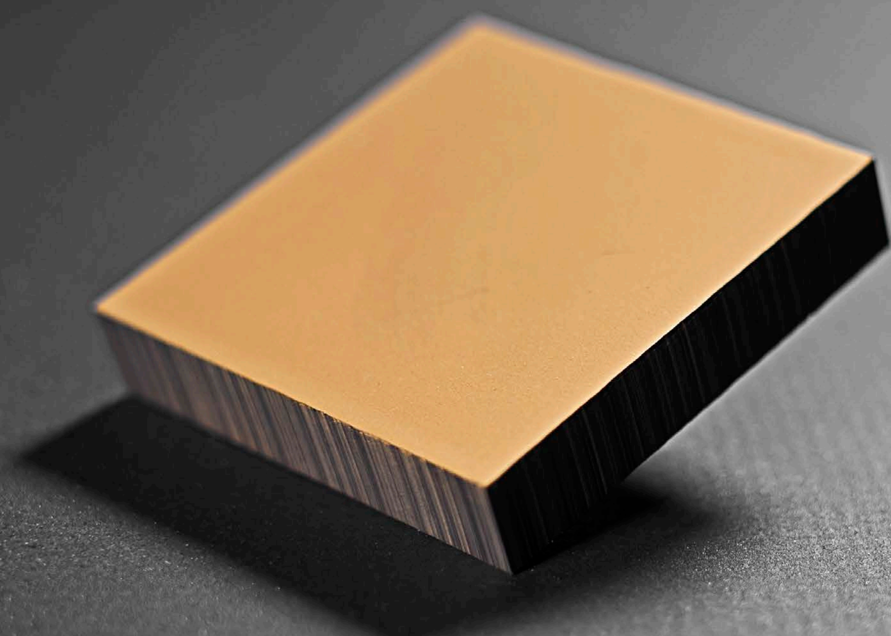
HIGH TEMPERATURE

AND CORROSION RESISTANT COATING

TACCOTA®



NIPPON KORNMEYER
CARBON GROUP

Fraunhofer
IISB

TACCOTA®

STABILIZES PROCESS
CONDITIONS IN SIC PVT
CRYSTAL GROWTH

250 MM
DIAMETER
PVT CRUCIBLE

HIGH TEMPERATURE AND CORROSION RESISTANT COATING

Nippon Kornmeyer Carbon Group GmbH and Fraunhofer IISB present their innovative and patented **tantalum carbide coating technology TACCOTA®.**

The high temperature and corrosion resistant coating can be applied to graphite substrates and used in semiconductor material production and processing. It secures graphite parts from decomposition and corrosion in typical high temperature and reactive gas processes like SiC and nitride PVT crystal growth and epitaxy, ion implantation, and plasma processing. The benefit is an increased lifetime and improved cost of ownership.

R&D BY FRAUNHOFER IISB:

- Delivery of test parts and application demonstrators
- Application testing support
- Custom tailored coating developments and short feedback loops
- R&D project collaboration

PARTS SUPPLY BY NIPPON KORNMEYER CARBON GROUP GMBH:

- From small batches to relevant production quantities

INCREASES THE LIFETIME
OF GRAPHITE PARTS IN
EPITAXY REACTORS

SCALABLE
UP TO 1000 MM
WITH THE TYPICAL
ROUGHNESS AND FLATNESS

ADVANCED COATING

IMPROVED SEMICONDUCTOR PROCESSES WITH REDUCED PRODUCTION COSTS

TECHNOLOGY BENEFITS

- Flexible for part size and geometry
- Part refurbishment possible
- Industry ready
- Environmentally friendly
- Free of conflict-affected materials

COATING FEATURES AND BENEFITS

- High temperature resistance / melting point (up to 3000° C)
- Resistance against corrosive gases and fluids, molten metals and salts
- Abrasion resistance and good adhesion to the substrate
- Avoidance of contact reactions
- Adjustable from porous to dense layers with different permeabilities
- Thickness between 20 - 200 µm possible

TACCOTA® COATING THICKNESS

FLEXIBILITY IN COATING PROPERTIES

The process technology allows the adjustment of the desired coating properties such as thickness and composition.

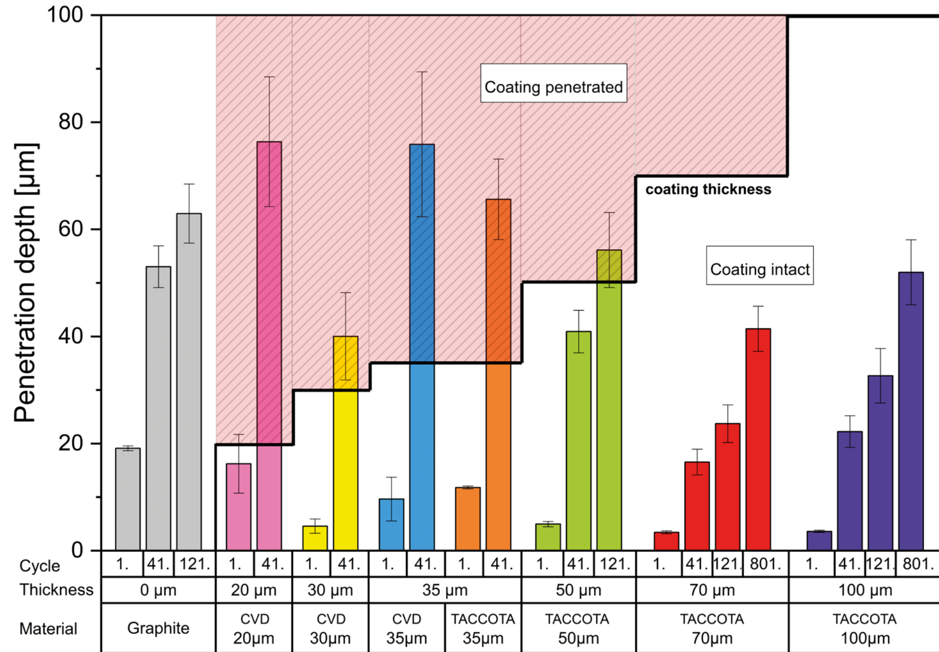
INCREASED COATING THICKNESS COMPARED TO CVD TAC COATING

DECREASED ROUGHNESS COMPARED TO CVD TAC COATING

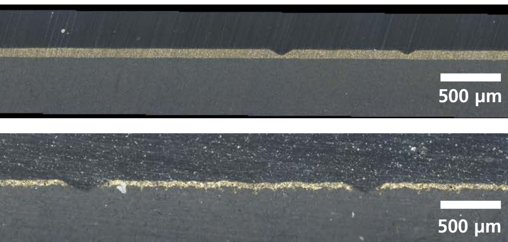
TACCOTA® MECHANICAL PROPERTIES

ABRASION RESISTANCE AND ADHESIVE STRENGTH

Scratch test results of TACCOTA® spray coating with variable thicknesses vs. CVD TaC coatings performed after DIN50324 / ASTM G99 and G133:



ENHANCED WEAR RESISTANCE DUE TO INCREASED COATING THICKNESS



- Cross cut test after DIN EN ISO 2409:2013-06 reveals that TACCOTA® is classified as ISO 0
- Pull off test after DIN EN ISO 4624:2014-06 showed 1.58 MPa adhesive strength before failure of the adhesive used for the measurements

TACCOTA® LOW-CONTAMINATION WAFER CARRIERS

- TANTALUM SURFACE CONTAMINATION IS INITIALLY ALWAYS BELOW 2E10 AT/CM² AND FURTHER DROPS WITH INCREASING EPI RUN NUMBER
- EVEN THE LOWER SIC WAFER SURFACE WHICH IS IN DIRECT CONTACT TO TACCOTA® SHOWS NO SIGNIFICANT CONTAMINATION (RUN #6)
- ALREADY 6 RUNS WITHOUT ANY DAMAGE OF THE CARRIER AND COATING DEMONSTRATED

TACCOTA® WAFER CARRIER BEFORE SIC EPITAXY RUN

TACCOTA® COATING PERFORMANCE UNDER SIC EPITAXY CONDITIONS

CHANGE WAFER CARRIER FROM CVD-TAC TO TACCOTA®

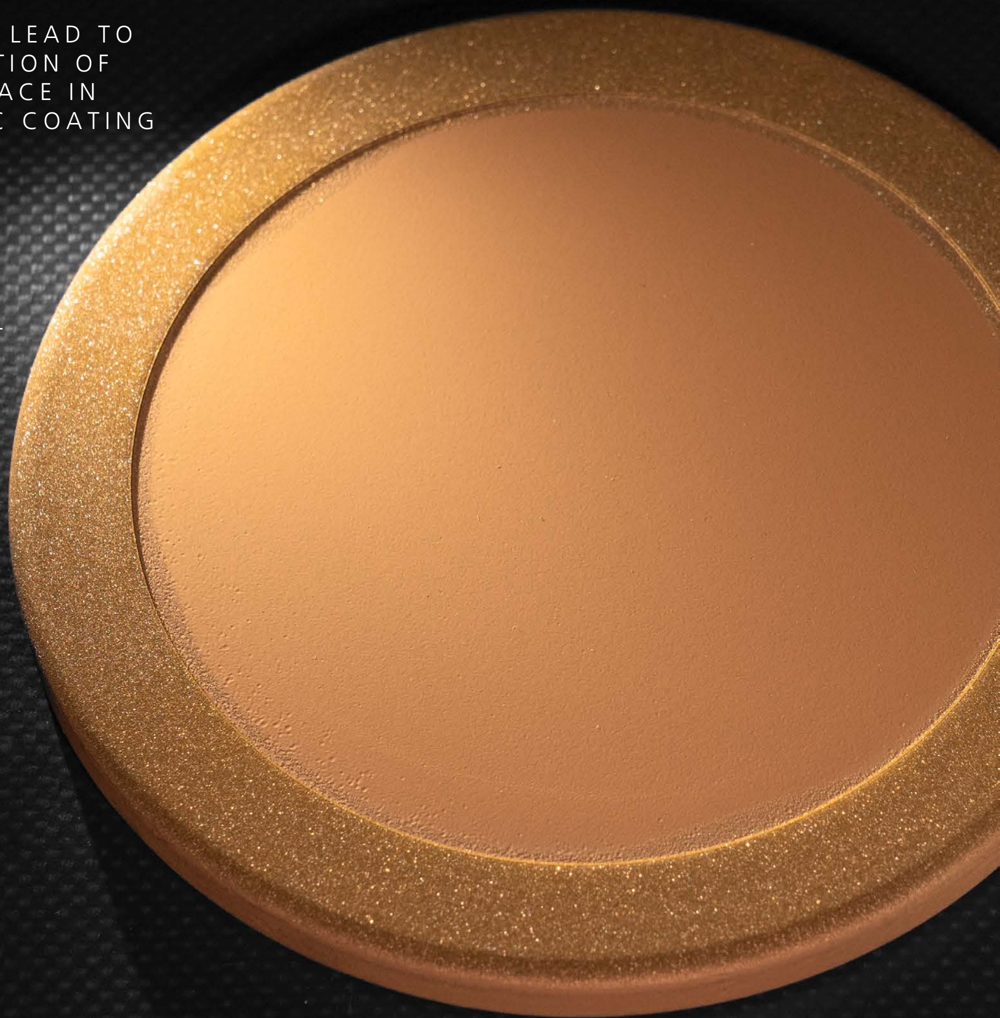
	Epi-Run	**#1**	**#2**	**#3**	**#4**	**#6**	**#9**	**Ref.**	**Ref.**
Detection limit (dl)	**Susceptor**	**CVD TaC**	**CVD TaC**	**CVD TaC**	**CVD TaC**	**CVD TaC**	**CVD TaC**	**Unused SiC wafer**	**Industry Epi reactor (CVD TaC)**
	Wafer carrier	**CVD TaC #1 (1st use)**	**CVD TaC #1 (2nd use)**	**CVD TaC #1 (3rd use)**	**TACCOTA #1 (1st use)**	**TACCOTA #1 flipped* (3rd use)**	**TACCOTA #1 (6th use)**		
0.065	**Li**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	n.m.
0.371	**Na**	<dl	<dl	4.536	6.204	0,908	<dl	1.068	n.m.
0.198	**Al**	2.570	<dl	<dl	0.499	6.700	3.555	<dl	n.m.
0.265	**K**	<dl	<dl	1.889	0.824	1.362	<dl	0.364	0.053
0.158	**Ca**	<dl	0.282	0.275	7.192	1.882	3.407	18.78	<dl (0.05)
0.125	**Ti**	<dl	<dl	<dl	0.292	0.141	<dl	<dl	<dl (0.03)
0.164	**V**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.02)
0.431	**Cr**	<dl	0.490	<dl	<dl	<dl	<dl	<dl	0.105
0.124	**Mn**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	0.488
0.375	**Fe**	<dl	2.575	<dl	<dl	<dl	<dl	<dl	0.306
0.062	**Co**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.02)
0.783	**Ni**	1.456	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.25)
0.551	**Cu**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.14)
0.206	**Zn**	<dl	<dl	0.233	<dl	<dl	<dl	<dl	<dl (0.05)
0.976	**As**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.21)
0.015	**Sr**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.003)
0.026	**Cd**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.004)
0.007	**Ba**	<dl	<dl	<dl	0.210	0.491	0.133	0.051	<dl (0.001)
0.002	**Ta**	119.0	71.98	5.101	1.854	0.932	0.174	0.066	0.058
0.010	**Pb**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.002)
0.037	**Bi**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.001)

Values for surface contamination in 1E10 at/cm², measured by VPD ICP-MS on Si-side of epi-ready Ø100 mm SiC-wafers. For each run, a virgin cleaned SiC-wafer was used with Si-side on top.

*In run #6, the SiC-wafer was intentionally flipped with Si-side in direct contact to TACCOTA® wafer carrier.

TACCOTA® LOW-CONTAMINATION WAFER CARRIERS

- WAFER CARRIERS DO NOT LEAD TO ADDITIONAL CONTAMINATION OF THE SIC WAFER TOP SURFACE IN COMPARISON TO CVD TAC COATING
- THE NUMBER OF FIRST EPI RUNS AFTER WHICH THE TANTALUM CONTAMINATION REACHES A NON-CRITICAL RANGE CAN BE REDUCED
- BY THE USE OF TACCOTA® SUSCEPTOR & WAFER CARRIER, THE INITIAL TANTALUM SURFACE CONTAMINATION ON THE SIC WAFER TOP SURFACE CAN BE REDUCED BY 75 %.



TACCOTA® WAFER CARRIER AFTER 6 SIC EPITAXY RUNS

TACCOTA® COATING PERFORMANCE UNDER SIC EPITAXY CONDITIONS

COMPLETE CHANGE FROM CVD-TAC TO TACCOTA®

	Epi-Run	#1	#2	#3	#10	#11	#12	Ref.	Ref.
Detec-tion limit (dl)	Susceptor	CVD TaC	CVD TaC	CVD TaC	TACCOTA	TACCOTA	TACCOTA	Unused SiC wafer	Industry Epi reactor (CVD TaC)
	Wafer carrier	CVD TaC #1 (1st use)	CVD TaC #1 (2nd use)	CVD TaC #1 (3rd use)	TACCOTA #2 (1st use)	TACCOTA #2 (2nd use)	TACCOTA #2 (3rd use)		
0.065	**Li**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	n.m.
0.371	**Na**	<dl	<dl	4.536	1.199	<dl	3.750	1.068	n.m.
0.198	**Al**	2.570	<dl	<dl	<dl	1.213	4.155	<dl	n.m.
0.265	**K**	<dl	<dl	1.889	0.847	<dl	3.183	0.364	0.053
0.158	**Ca**	<dl	0.282	0.275	4.850	1.766	<dl	18.78	<dl (0.05)
0.125	**Ti**	<dl	<dl	<dl	0.229	<dl	0.664	<dl	<dl (0.03)
0.164	**V**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.02)
0.431	**Cr**	<dl	0.490	<dl	<dl	<dl	<dl	<dl	0.105
0.124	**Mn**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	0.488
0.375	**Fe**	<dl	2.575	<dl	<dl	<dl	<dl	<dl	0.306
0.062	**Co**	<dl	<dl	<dl	<dl	<dl	0,265	<dl	<dl (0.02)
0.783	**Ni**	1.456	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.25)
0.551	**Cu**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.14)
0.206	**Zn**	<dl	<dl	0.233	0.178	0.075	0.150	<dl	<dl (0.05)
0.976	**As**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.21)
0.015	**Sr**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.003)
0.026	**Cd**	<dl	<dl	<dl	<dl	<dl	<dl	<dl	<dl (0.004)
0.007	**Ba**	<dl	<dl	<dl	0.180	0.234	0.128	0.051	<dl (0.001)
0.002	**Ta**	119.0	71.98	5.101	26.67	5.977	0.269	0.066	0.058
0.010	**Pb**	<dl	<dl	<dl	0.022	<dl	<dl	<dl	<dl (0.002)
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Values for surface contamination in 1E10 at/cm², measured by VPD ICP-MS on Si-side of epi-ready Ø100 mm SiC-wafers. For each run, a virgin cleaned SiC-wafer was used with Si-side on top.

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